PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTEREFERENCES

In re Application of:

Hill et al.

Serial No.: 10/067,410

Filed: February 4, 2002

For: METHOD FOR FORMING A SELECTIVE CONTACT AND LOCAL INTERCONNECT IN SITU (as amended)

Confirmation No.: 8302

Examiner: H. Lee

Group Art Unit: 2823

Attorney Docket No.: 2269-3380.1US

VIA ELECTRONIC FILING
November 19, 2008

REPLY BRIEF

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Attn: Board of Patent Appeals and Interferences

Sirs:

This REPLY BRIEF, which is being submitted pursuant to 37 C.F.R. § 41.41, follows the Examiner's Answer of September 19, 2008, the statutory period for response to which expires on November 19, 2008.

VII. ARGUMENT

The Examiner has based all of his rejections upon the subject matter taught by U.S. Patent 6,020,259 to Chen et al. (hereinafter "Chen"). Chen teaches a process in which titanium silicide ($TiSi_2$) is deposited by chemical vapor deposition (CVD) processes and, thereafter, CVD is used to deposit titanium nitride (TiN). As the Examiner has acknowledged, Chen does not teach or suggest that the $TiSi_2$ and TiN deposition processes may be effected *in situ*. Examiner's Answer, page 11.

For this reason, the Examiner has had to assert that "it is conventional practice to perform as many processing steps in a single apparatus as possible to avoid contamination from the outside atmosphere." Examiner's Answer, page 11. Unfortunately, the Examiner has overlooked the fact that he "bears the initial burden of *factually supporting* [his] *prima facie* conclusion of obviousness" (M.P.E.P. § 2142, emphasis supplied), and has not proffered any prior art that supports the assertion that depositing a contact material and an interconnect material *in situ* would have been "conventional practice."

The Examiner's assertion also overlooks the fact that the highly controlled clean room environment in which semiconductor devices are fabricated itself minimizes the potential for contamination as semiconductor substrates (*e.g.*, silicon wafers, etc.) are transported from one process station (*e.g.*, on CVD chamber, etc.) to another.

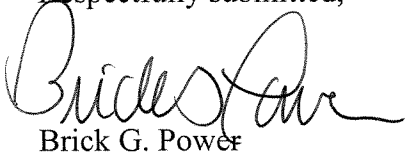
Furthermore, the Examiner's assertion that it would have been obvious to deposit $TiSi_2$ and TiN *in situ* begs the question: if it was so obvious, why didn't Chen or anyone else teach or suggest that $TiSi_2$ and TiN could be deposited *in situ* before the earliest date to which a claim for priority has been made in the above-referenced application? The answer to that question is itself

obvious: the Examiner has not been able to locate any prior art that supports his assertion.

Without any prior art that teaches or suggests that a contact material (*e.g.,* $TiSi_2$, etc.) and an interconnect material (*e.g.,* TiN, etc.) could be deposited *in situ*, the Examiner has not met the burden that has been placed upon him in establishing a *prima facie* case of obviousness against independent claim 1, independent claim 20, or any of their dependent claims. It is, therefore, respectfully submitted that, under 35 U.S.C. § 103(a), each of claims 1-28 is allowable over the subject matter taught by Chen, when taken alone or in combination with teachings from any of the other references that have been relied upon in the final claim rejections that have been presented by the Examiner.

Accordingly, it is respectfully requested that the 35 U.S.C. § 103(a) rejections of claims 1-28 be reversed.

Respectfully submitted,



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